CLAIMS

1	1.	A multi-layer assembly comprising:
2		a first silicon layer comprising at least first and second surfaces, and further
3		comprising a structure that transitions from an amorphous silicon region adjacent to
4		the first surface, to a polysilicon region adjacent to the second surface;
5	-	a second layer adjacent to the first surface of the first layer; and
6	٠.	a third layer adjacent to the second surface of the first layer; wherein
7		at least one of the second and third layers comprises a dielectric.
1	2.	A multi-layer assembly comprising:
2		a first silicon layer comprising at least first and second surfaces, and further
3		comprising a structure having a first region composed of amorphous silicon adjacent
4		to the first surface, a second region composed of polysilicon adjacent to the second
5		surface, and an intermediate region between the first and second regions, the
6		intermediate region comprised partially of amorphous silicon and partially of
7		polysilicon;
8		a second layer adjacent to the first surface of the first layer; and
9		a third layer adjacent to the second surface of the first layer; wherein
0		at least one of the second and third layers comprises a dielectric.
1	3.	A multi-layer assembly as in claim 2, wherein the intermediate region has a
2		continuous phase distribution from amorphous silicon to polysilicon.
1 .	4.	A semiconductor device having a floating gate, the floating gate comprising a silicon
2		structure having at least first and second surfaces and transitioning from an
3		amorphous silicon region adjacent to the first surface to a polysilicon region adjacent
4		to the second surface.
1	5.	A semiconductor device having a floating gate, the floating gate comprising a silicon
2		structure having at least first and second surfaces;
3		the structure comprising at least first and second regions;
4		the first region comprising amorphous silicon, and adjacent to the first surface;
5		and

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O	the second region comprising polysilicon, and adjacent to the second surface.
1	6. A semiconductor device as in claim 5, wherein the silicon structure further comprises
2	an intermediate region between the first and second surfaces, wherein the
3	intermediate region has a phase distribution that transitions from amorphous silicon
4	to polysilicon.
1	7. A method of forming a layer on a substrate, comprising:
2	depositing a silicon layer on the substrate; and
3	controlling the temperature during the step of depositing the silicon layer,
4	from a starting temperature favoring the formation of polysilicon, to an ending
5	temperature favoring the formation of amorphous silicon.
1	8. A method as in claim 6, wherein:
2	the starting temperature is approximately 620°C; and
3	the ending temperature is in a range from about 500°C to about 550°C.
1	9. A method of forming a floating gate on a semiconductor substrate, comprising:
2	forming a first dielectric layer on the semiconductor substrate;
3	depositing a silicon layer superposing the first layer;
4	forming a second dielectric layer superposing the silicon layer; and
5	controlling the temperature during the step of depositing the silicon layer,
6	from a starting temperature to an ending temperature, wherein the starting temperature
7	is higher than the ending temperature.
1	10. A method as in claim 9, wherein:
2	the starting temperature is selected to form a polysilicon region adjacent to the
3	first dielectric layer; and
4	the ending temperature is selected to form an amorphous silicon region
5	adjacent to the second dielectric layer.
1	11. A method as in claim 10, wherein:
2	the starting temperature is approximately 620°C; and
3	the ending temperature is in a range from about 500°C to about 550°C.